EE 310 - Hardware Description Languages*
Spring 2023 - 2024

Instructors Information

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Office Hours:	By appointment	Monday 09:00-11:00

Schedule

Lecture:	Wednesday	14:40 - 17:30	Online
Lab:	Thursday	18:40 - 19:30	FENS 1033

https://sabanciuniv.zoom.us/j/97418092685?pwd=Y2M5ZVBQendWRHNqdE9wZVlXbi83dz09

Course Information

This course introduces modeling digital circuits using Hardware Description Languages (HDL). It then introduces Verilog HDL and covers behavioral modeling and verification of digital circuits using Verilog HDL. It then covers RTL modeling with Verilog and logic synthesis to standard cell libraries and FPGAs. In this course, students will also gain practical design experience by using Xilinx Vivado CAD tools to design and implement several digital circuits.

Tentative Outline

- **Introduction and Digital design with HDLs**
- **Verilog Language Elements**
- **Gate-level Modeling with Verilog**
- **Behavioral Modeling with Verilog**
- **Simulation with Verilog**
- **Logic Synthesis, Standard cell libraries**
- **Field Programmable Gate Arrays**
- **RTL Modeling with Verilog**
- **Verilog RTL Mdel Optimizations**
- **Design verification**

*All information in this document is tentative. The instructors reserve the right to make changes in the semester.

Textbook

Jayaram Bhasker, A Verilog HDL Primer. Star Galaxy Publishing, 2005, 3rd Edition.
Jayaram Bhasker, Verilog HDL Synthesis: A Practical Primer. Star Galaxy Publishing, 1998.

References

Samir Palnitkar, Verilog HDL: A Guide to Digital Design and Synthesis. 2nd Edition , Prentice Hall, 2003.

IEEE Std 1364-2005 (Revision of IEEE Std 1364-2001), IEEE Standard for Verilog Hardware Description Language, 2006.

Student Responsibilities

- **Exams:** Students are required to comply with instructor's rules for exams (midterm, and final)
- **Labs:** There will be about 5 (± 1) Lab assignments.
- **Term project:** Students are required to work on a term project. It is essential for students to meet time schedule of the projects. Project groups must provide a demonstration/presentation of their work. During the demonstration/presentation, all the project members must be present. Students may work in groups of two.
- **Quizes:** Students are required to attend pop-quizes which will be assigned during the lectures.

Tentative Grading

- Midterm Exam 25%
- Final Exam 30%
- Term Project 15%[1][2]
- Labs (Total 5(± 1)) 25%[3][4]
- Quizes 5%

Midterm Exam and Final Exam will be held in-person.

[1] The highest grade you can get from term project is **2** times of your weighted exam average. For example, if your weighted exam average is 40%, then maximum of each take-home exam grade is 80% even if you get more than that.

[2]
$$WeightedExamAverage = \frac{(Midterm \times 0.25) + (Final \times 0.3)}{0.55}$$

[3] The highest grade you can get from an individual lab assignment is **2** times of your weighted exam average. For example, if your weighted exam average is 40%, then maximum of each lab grade is 80% even if you get more than that.

[4] See footnote 2

Exam Dates

Midterm:	TBA
Final:	will be scheduled by SR

Make-up Policy

- There will be no make-up for Labs, Term Project, and Quizes. Students automatically get 0 (zero) from the respective assignment grade if any of them is missed.
- Make-up is only allowed for the midterm and final examinations to those with an official medical report and to those with an official permission notice from the university on the date of the exam in question.
- Make-up examinations may be written and/or oral.

Time Conflict Permission Policy

In general, time conflict permission requests are approved in this course [5]. However, time conflict permission is not a permission for you not to attend some classes. Moreover, it does not mean that, time conflicts will be taken into account when planning any activity (exam, quiz, etc.) for the corresponding hour. The conflicted hour as an hour that you have reserved only for this course like other students who do not have a time conflict. It is the responsibility of the student, who took time conflict permission, to manage potential problems that may arise due to time conflict.

It is assumed that the students, who are registered to this course with time conflict permission, accept these terms.

Plagiarism Policy (Academic Integrity)

Plagiarism means presenting someone else's work as yours. This is a very serious and ethical problem. A plagiarized work may or may not be a verbatim copy of another submission. Verbatim copies are of course plagiarized ones. However, if a submission is derived from another one by partially changing some parts, this action is also plagiarism. When a plagiarism case is detected, sanctions are applied to all parties regardless of the actual source of the submission. These sanctions are as follows:

- For the midterm/final examinations,
  - students directly fail the course, even in the first offense.[6]
- For the Labs,
  - for the first time, all plagiarized submission owners receive -100,
  - the second time, the student fails the course automatically. [7]

[5] The instructors reserve the right to reject any request.

[6] Additionally, the case will be referred to the FENS Dean's Office for disciplinary action. This course does not tolerate any breach of academic integrity (more info on https://www.sabanciuniv.edu/en/academic-integrity-statement)

[7] See footnote 6