

EE302 – Digital Integrated Circuits

Sabanci University, 2022-2023 Spring

Disclaimer: We may have to revise the course plan according to the countrywide reassessment regarding higher education, and this is expected to happen at the beginning of April. The course delivery method, the number and dates of exams, and other details are subject to change. Note that we are not going to sacrifice the content.

Instructor: Korkut Kaan Tokgoz, korkut.tokgoz@sabanciuniv.edu
Office Hours: Online or face-to-face: Communicate first with e-mail (Office: FENS1064)
Teaching Assistant: Hossein Mahdavi, hmahdavi@sabanciuniv.edu
Grading Policy: **Homework 20%, Midterm 15%, Labs 30%, Final 35%**
The midterm will be around mid to late April.
Cheating and late submissions are severely penalized.

Lectures: Tuesdays 12:40-14:30 FENS L035
<https://sabanciuniv.zoom.us/j/99843967475?pwd=SWNuMIJmNWZaNmFvQUpmY3BQblVsQT09>
Wednesdays 08:40-09:30 FENS L030

<https://sabanciuniv.zoom.us/j/91515680791?pwd=NUs5L2hoRHgxd2lMMFZRM3gway9mQT09>
Labs: Online: Fridays 12:40-14:30
<https://sabanciuniv.zoom.us/j/4888488960>

Tentative Outline:

Week	Topic
#1	Introduction to Digital IC Fundamentals
#2&3	Static and Dynamic Operation of CMOS Inverters
#4&5	Static CMOS Logic Gates
#6&7	Sequential Logic Gates
#8&9	Dynamic Logic
#10-12	Memory Cells/Arrays
#13	Power Management (if time permits)

Labs: Implementation of standard cell designs using Cadence (Inverter, NOR, NAND, Flip Flops, SRAM).

Computer Usage: Cadence Software under CentOS Linux.

Class Policy: Regular attendance is essential and expected.

Recommended Textbooks: Note that these are recommended, not strictly followed.

1. CMOS Digital Integrated Circuits by S. Kang, Y. Leblebici, 3rd Ed., McGraw-Hill, 2003.
2. Digital Integrated Circuits: A Design Perspective by J. M. Rabaey, Prentice Hall, 2003.

Other Relevant Material: Cadence tutorial at <http://acoustics.sabanciuniv.edu/cds/>