

# SABANCI UNIVERSITY

## Faculty of Engineering & Natural Sciences

### EE 401 – Very Large Scale Integrated System Design I

### EE 58003-0 – Special Topics in EE: VLSI Systems Design I

### Fall 2024/2025 Syllabus

#### **Instructor**

Ömer Ceylan

[omer.ceylan@sabanciuniv.edu](mailto:omer.ceylan@sabanciuniv.edu)

**Office Hours:** TBD

#### **Teaching Assistant**

Oğuz Çınar (cinaroguz@sabanciuniv.edu)

Mahmut Melih Özkan  
(omelih@sabanciuniv.edu)

**Zoom Link:** <https://sabanciuniv.zoom.us/j/9757380583>

**Zoom Meeting ID:** 975 738 0583

#### **Class Schedule**

##### **Lectures**

**Monday:** 9:40 – 11:30 FENS L048

**Thursday:** 16:40 – 17:30 FASS 1096

##### **Recitation / Lab**

**Thursday:** 17:40 – 18:30 FENS L030

#### **Textbooks**

CMOS VLSI Design: A Circuits and Systems Perspective (4th Edition), Neil Weste and David Harris, Addison-Wesley

Digital Interated Circuits – A Design Perspective (2nd Edition), Jan M. Rabaey, Anantha Chandrakasan and Borivoje Nikolic, Prentice-Hall

#### **Course Content:**

Complementary Metal-Oxide Semiconductor (CMOS) technology and limitations; CMOS circuit and logic design; layout rules and techniques; circuit characterization and performance

estimation; Very-Large-Scale Integrated (VLSI) system design methods; synthesis, place & route, physical verification, logic and circuit simulation.

### **Learning Outcomes:**

- Describe digital VLSI circuit design styles;
- Analyze and reduce delay of full custom digital VLSI circuits;
- Design and analyze full custom arithmetic circuits (e.g. adder, multiplier);
- Describe basic techniques for reducing power consumption of digital VLSI circuits;
- Describe clock generation and distribution in synchronous digital VLSI circuits;
- Describe standard cell libraries;
- Design and implement standard cell based digital VLSI circuits using logic synthesis and physical synthesis tools;
- Verify functionality and timing of standard cell based digital VLSI circuits using a logic simulation tool.
- Physical verification of VLSI circuits

### **Tentative Course Schedule:**

<b>Date</b>	<b>Subjects</b>
Week 1-2	Introduction
Week 3-4	Adders / Shifters / Multipliers
Week 5	CMOS Delay Estimation
Week 6-7	Synthesis
Week 8-9	Midterm / Timings / Clocks
Week 10	Floorplanning & Placement
Week 11	Clock Tree Synthesis
Week 12-13	Routing
Week 14	Packaging & I/O

### **Course Policies:**

- Cheating will not be tolerated.
- For homeworks, labs and projects late submission is penalized up to 2 days.
  - Up to 24 hours late 25% reduction
  - Up to 48 hours late 50% reduction

## **Grading Policy:**

Attendance	5%
Labs / Projects	30%
Midterm	30%
Final	35%

## **Important Notes:**

- For proctored exams, your webcam and microphone should be on during the exam. In the case of non-compliance with this and other declared exam procedures, your exam will be void. Make sure to check that your webcam and microphone function properly before the exam.
- You may be given an oral exam to check the authenticity of the written exam by going through the questions of the written exam.
- You must attend the synchronous Zoom lectures, recitations, etc. and real-time online exams with your SU email account.